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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Roger Lewis — Examiner: Leonid Shapiro

Serial No.: 09/834276 — Group Art Unit: 2673

Filed: April 12, 2001 — Docket: H26651 (256.161US1)

For: METHOD, APPARATUS AND COMPUTER PROGRAM PRODUCT FOR CONTROLLING LED BACKLIGHTS AND FOR IMPROVED PULSE WIDTH MODULATION RESOLUTION

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on December 29, 2003, from the Final Rejection of claims 1-12, 14-19 and 21-23 of the above-identified application, as set forth in the Final Office Action mailed on September 12, 2003.

This Appeal Brief is filed in triplicate. The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 330.00 which represents the requisite fee set forth in 37 C.F.R. § 117. The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, HONEYWELL INTERNATIONAL INC.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-12, 14-19 and 21-23 are pending in the application and have all been finally rejected. The rejected claims 1-12, 14-19 and 21-23 are the subject of the present appeal.

4. STATUS OF AMENDMENTS

An amendment of October 13, 2003 subsequent to the Final Office Action mailed to the Appellants on August 13, 2003 contained minor changes to the specification, but no claim amendments. The amendment was considered by the Examiner as reflected in the Advisory Action mailed November 5, 2003.

5. SUMMARY OF THE INVENTION

An additional timer 918 is provided with a pulse width modulator 916 that provides the ability to control a duty cycle provided by the pulse width modulator with a higher resolution than is available from the unmodified pulse width modulator. The timer is used to define multiple states (FIG.s 5A and 5B) for the modulator. The modulator is then set to provide selected pulses for each of the states, which are then repeated. This allows finer resolution duty cycle for a pulse width modulator with limited resolution as described at page 8, line 20 et seq.

In one embodiment, a method utilizes a hardware based pulse width modulator 918

having a limited range of output signals it can generate. The method is used to generate a pulse width modulated signal during a first time interval having a first modulator output. Multiple further pulse width modulated signals are generated during multiple succeeding time intervals having selected modulator outputs. The generation of such pulse width modulated signals during the first and succeeding time intervals is repeated to provide an overall duty cycle having a desired resolution higher than the resolution of the hardware based pulse width modulator. See the paragraph beginning on page 8 at line 20.

In one embodiment, the pulse width modulator has n bits of resolution and a nominal time period P_n. The additional timer is provided with a timer period P_T. The addition timer generates multiple (K) associated states, with K being greater than 2. A modulator output value is associated with each one of the K states. A pulse width modulation update interval of $K*P_T$ is established. As seen in FIG.s 5A and 5B, this can result in a different duty cycle every state or timer period when K is one. As the states are cycled through, it provides an effective increase in the resolution of the pulse width modulator beyond its n bits of resolution, allowing more variation in the duty cycle of the pulse width modulator. In general, the duty cycle can be expressed as the ratio of the pulse "on" time to the total period. This is described in the detailed description starting at page 5, line 21. Block 718 in FIG. 7 references setting the pulse width modulation to an appropriate value for a state.

In one embodiment, the additional timer period P_T is an integer multiple of the pulse width modulator nominal time period P_n. The pulse width modulator may include an overflow bit. A computing device assigns a modulator output value to each of said K states in a further embodiment. The invention includes apparatus, method and computer program product embodiments. In a further embodiment, a pulse is outputted according to the modulator output value during each time period P_n occurring within said timer period P_T during each one of said K timer states, whereby the resolution of said n bit pulse width modulator substantially equals n + log2(K). In a further embodiment, P_T is other than an integer multiple or P_n. An example of this

is shown in FIG. 7 of the present application.

In a further embodiment, the resolution of a hardware based pulse width modulator is increased by specifying a desired duty cycle and determining a timer state. If the state needs to be set at 100% duty cycle, the duty cycle is set to 100%. Otherwise the pulse width modulation of the pulse width modulator is set to an appropriate value for this state, and a 100% duty cycle bit is turned off. A state counter is then incremented for a next state.

6. ISSUES PRESENTED FOR REVIEW

Whether claims 21-23 are enabled by the specification under 35 USC §112, first paragraph.

Whether claims 1-2, 4-6, 8-9, 11-12, 14-17 and 19 are patentable over Zuraski et al. (US 5,589,805) in view of Akiko (JP 04-096417).

Whether claims 3, 7, 10 and 18 are patentable over Zuraski et al. (US 5,589,805) and Akiko (JP 04-096417), and further in view of Shibuya et al. (US 6,191,868).

7. GROUPING OF CLAIMS

Claims 1-4 are grouped together for purposes of appeal and are argued separately from other groups.

Claims 5-8 are grouped together for purposes of appeal and are argued separately from other groups.

Claims 9, 10, 17 and 18 are grouped together for purposes of appeal and are argued separately from other groups.

Claims 11-12 are grouped together for purposes of appeal and are argued separately from other groups.

Claims 14-16, and 19 are grouped together for purposes of appeal and are argued separately from other groups.

Claims 21-23 are grouped together for purposes of appeal and are argued separately from other groups.

8. ARGUMENT

I) Rejection under 35 U.S.C. § 112, first paragraph

a) The Applicable Law

35 U.S.C. § 112, first paragraph states:
"The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor carrying out his invention."

As described in MPEP § 2164 et seq.: "A patent need not teach, and preferably omits what is well known in the art. In re Buchner, 929 F. 2d 660, 661, 18 USPQ 2d 1331, 1332 (Fed. Cir. 1991)..." 37 CFR § 1.83(a) further points out: "However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box)."

b) Discussion of the Rejection

Claims 21-23 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This rejection is respectfully traversed. A hardware based pulse width modulator is clearly described with respect to Fig. 10, starting at page 10, line 26, describing an LED backlight and associated drive electronics. Pulse width modulator 916 is represented by a block because such modulators are well known. This is consistent with the background of the invention on page 5, where a specific reference to known hardware pulse width modulators is included:

"Absent the present invention, the only way to achieve the desired resolution is to change the pulse width modulator to one having three bit or higher resolution. Changing the **hardware** in such fashion may be impractical because the desired hardware is unavailable or costly due to the associated hardware and software changes." Emphasis added. Thus, known hardware has been described and represented as a block. Including details of implementation as suggested in the advisory action mailed November 5, 2003 would be inconsistent with the wording of MPEP § 2164, which indicates that such details should be omitted.

Since this was the only rejection of these claims, it is respectfully requested that the rejection be reversed, and the claims allowed.

II) Rejections under 35 U.S.C. § 103

a) The Applicable Law

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.*

The M.P.E.P. contains explicit direction to the Examiner that agrees with the court in *In re Fine*:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). At the same time, however, although it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d (BNA) 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. (BNA) 171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an innovator but rather that of the person who follows the conventional wisdom in the art. *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 474, 227 U.S.P.Q. (BNA) 293, 298 (Fed. Cir. 1985).

The Federal Circuit, in the recently decided *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002), reiterated the prior cases and specifically required that

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching motivation or suggestion to select and combine the references relied on as evidence of obviousness" 61 USPQ2d at 1433.

The Federal Circuit in *In re Lee* also indicated that the "factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority." 61 USPQ2d at 1434.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). The Examiner can only rely on references which are either in the same field as that of the invention, or if not in the same field, must be "reasonably

pertinent to the particular problem with which the inventor was concerned." *M.P.E.P.* § 2141.01 (a) (citing *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443 at 1445). The Examiner must also recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990). Furthermore, if the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)). Finally, the Examiner must avoid hindsight. *Id.* The Examiner cannot use the Applicant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991).

b) Discussion of the Rejection

Claims 1-2, 4-6, 8-9, 11-12, 14-17, 19 were rejected under 35 USC § 103(a) as being unpatentable over Zuraski et al. (U.S. Patent No. 5,589,805) in view of Akiko (JP 04-096417). This rejection is respectfully traversed on the basis that Zuraski et al. and Akiko either alone or combined do not show, teach or suggest each and every element of the invention as claimed.

Zuraski et al. indicates that "a predetermined control period (T_c) provides regular intervals of adjustment for the PWM_n output state in accordance with a set of program instructions not germane to the present invention nor necessitating further discussion herein", at Col. 5, lines 9-12. Thus, Zuraski et al. clearly lacks the last element of claim 1: "establishing a pulse width modulation update interval of $K*P_T$." The update interval is clearly a function of the number of additional states. Zuraski et al., only "toggles between two adjacent output states during any single control period" (Abstract) or said in a different manner: "varies between adjacent discrete PWM_n output states, (s) and (s + 1) within such control period T_c" Col. 5, lines

19-21. The presently claimed invention in claim 1 recites "associating a modulator output value with each one of the said K states", "wherein K is greater than 2", which allows multiple different states during a time period that is a function of the additional states.

The Examiner agrees that Zuraski et al. does not show an additional timer to generate K associated states, wherein K is greater than 2 and establishing a pulse width modulation update interval $K*P_T$. It is then stated that "Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (See Figs. 2, 5, items 1-2 in Detailed Description See Page 1, last paragraph and Page 3, 1st paragraph)." The implications of this characterization are respectfully traversed. The timer is part of the PWM, not an additional timer as claimed.

Akiko, in the translation provided, states that when the timer register value is equal to a value in a comparison register at the bottom of page 1, a timer interrupt is generated and PWM output is carried out. No additional timer is used to generate K additional states. Rather, a comparison register appears to be used to modify the PWM at the end of each timer period of the PWM. The timer in Akiko appears to be part of the PWM. This is further supported by the language in Akiko indicating that the timer and PWM resolution are both 8 bits, and that the overall resolution is increased "n" times due to the averaging of multiple PWM outputs. Thus, while both the claimed invention and Akiko increase resolution of the PWM, they do so in a different manner. Akiko uses a comparison register, while the currently claimed invention uses an additional timer to define multiple states.

Akiko also does not describe the pulse width modulation update interval that is claimed. Page 3 of Akiko indicates that the table of Figure 2 contains the average values of the values set in the comparison register. Average values do not teach or suggest establishing a pulse width modulation update interval $K*P_T$ as claimed. Thus, since the combination of the references do not teach or suggest each and every element of claim 1, the rejection should be reversed.

The Final Office Action indicates that "It would have been obvious to one or ordinary skill in the art at the time of the invention to use timer with K greater than 2 as shown by Akiko

in the Zuraski et al. method..." As indicated above, Akiko does not show such a timer. As such, the rejection is believed improper and should be reversed.

Claims 2-4 depend from claim 1 and are believed allowable at least for the same reasons. The further reference cited with respect to some of these claims does not provide the missing elements.

Claim 5 recites "outputting a pulse according to said modulator output value during each time period P_n occurring within said timer period P_T during each one of said K timer states". This is clearly not provided by Zuraski et al., nor Akiko as previously described. Claims 6-10 depend from claim 5 and are believed allowable for at least the same reasons.

Claims 9 and 17 include a P_T other than an integer multiple of P_n. An example of this is shown in FIG. 7 of the present application. The Final Office Action merely indicates that "It would have been obvious to one of ordinary skill in the art at the time of the invention to use external clock to the timers of the microprocessor to have Pt other than integer multiple of Pn in the Zuraski et al. method." This statement is unsupported. Zuraski et al. toggles between adjacent states. There is no hint of any suggestion in either reference at any concept of having an additional timer period that is a non-integer multiple of the nominal pulse width modulator period. Since the basis of the rejection of claims 9 and 17, and dependent claims 10 and 18, is unsupported, the rejection should be reversed.

Claim 11, along with dependent claim 12 also contain a recitation about assigning a modulator output value with each one of said "K states, wherein K is greater than 2, with a timer having a period P_T;". As with claim 1, the references do not teach or suggest such a timer. Since elements of the claims are written in a means plus function format, they are interpreted to include the structure that accomplishes the function described in the application and equivalents thereof. This structure corresponds to the structure in FIG. 10, and its functions described with respect to the remaining Figures. In particular, it includes the multiple additional states used within a period P_T, which is a multiple of the PWM period. Even if not interpreted as means plus

function claims, the elements recited clearly distinguish the references. A third means "assigns an n bit modulator output value with each one of said K states according to said duty cycle." None of the references teach or suggest this, and the rejection should be reversed.

Claim 14 also recites a timer to generate K timer states, wherein K greater than 2, and the outputting of a plurality of pulses according to modulator output values to obtain a resolution dependent on K. Thus, it clearly distinguishes over the references, since Zuraski et al. only utilizes adjacent output states during a period, and both Zuraski et al., and Akiko also lack an additional timer. Claims 15-18 depend from claim 14, and are believed allowable for at least the same reasons.

Claim 19 is similar to claim 14 and is allowable for at least the same reasons.

Claims 3, 7, 10, 18 were rejected under 35 USC § 103(a) as being unpatentable over Zuraski et al. and Akiko as aforementioned in claims 1, 5, 14 in view of Shibuya et al. (U.S. Patent No. 6,191,868). These claims are believed allowable as indicated above since they depend from claims that are believed allowable, and Shibuya et al. does not provide the element or elements missing from Zuraski et al. and Akiko.

9. SUMMARY

Appellant respectfully submits that the art cited does not render the claimed invention obvious and that therefore the claimed invention does patentably distinguish over the cited art. It is respectfully submitted that claims 1-12, 14-19 and 21-23 should therefore be allowed. Reversal of the Examiner's rejections of claims 1-12, 14-19 and 21-23 is respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also respectfully requested.

Respectfully submitted,

ROGER LEWIS

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402

Date 2-27-2004 By _____
Bradley A. Forrest
Reg. No. 30,837

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 27 day of February, 2004.

Gina M. Uphus _____
Name Signature

APPENDIX I

The Claims on Appeal

1. (Previously Presented) A method for pulse width modulation comprising the steps of:

providing a pulse width modulator having n bits of resolution and a nominal time period P_n;

supplying an additional timer to generate K associated states and having a timer period P_T, wherein K is greater than 2;

associating a modulator output value with each one of said K states; and

establishing a pulse width modulation update interval of $K*P_T$.

2. (Original) The method of claim 1 wherein P_T is an integer multiple of P_n.

3. (Original) The method of claim 1 wherein said pulse width modulator includes an overflow bit.

4. (Original) The method of claim 1 wherein $P_T = P_n$.

5. (Previously Presented) A method for improving the resolution of an n bit pulse width modulator having a nominal time period of P_n, the method comprising the steps of:

supplying an additional timer having K associated states, wherein K is greater than 2, and a timer period of P_T;

associating a modulator output value with each one of said K states; and

outputting a pulse according to said modulator output value during each time period P_n occurring within said timer period P_T during each one of said K timer states, whereby the resolution of said n bit pulse width modulator substantially equals n + log2(K).

6. (Original) The method of claim 5 wherein P_T is an integer multiple of P_n.

7. (Original) The method of claim 5 wherein said pulse width modulator includes an overflow bit.

8. (Original) The method of claim 5 wherein $P_T = P_n$.

9. (Original) The method of claim 5 where P_T is other than an integer multiple of P_n and $P_T >> P_n$.

10. (Original) The method of claim 9 wherein said pulse width modulator includes an overflow bit.

11. (Previously Presented) A computer program product for pulse width modulation comprising:

a computer readable storage medium having computer readable program code means embedded in said medium, said computer readable program code means having:

a first computer instruction means for associating K timer states, wherein K is greater than 2, with a timer having a period P_T; and

a second computer instruction means for reading a commanded pulse width modulation duty cycle;

a third computer instruction means for assigning an n bit modulator output value with each one of said K states according to said duty cycle.

12. (Original) The computer program product of claim 11 wherein said third computer instruction means updates said n bit modulator output value assigned to each state at time intervals of $K*P_T$.

13. (Withdrawn) A method for controlling the brightness of a display using pulse width modulation comprising the steps of:

receiving a commanded brightness level;

using an n bit pulse width modulator to assert a plurality of pulses in accordance with an output of said n bit pulse modulator wherein said modulator has a period P_n;

assigning a modulator output value to each one of K states of a K state timer wherein said timer has a period P_T;

outputting said plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T; and

supplying power to the display in accordance with said plurality of pulses.

14. (Previously Presented) An apparatus for pulse width modulation comprising:

an n bit pulse width modulator having a nominal modulator period P_n;

a timer to generate K timer states, wherein K is greater than 2, and having a timer period P_T;

a computing device for assigning a modulator output value to each of said K states; and

whereby said modulator outputs a plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T and whereby said pulse width modulator has a resolution of $n + \log_2 K$.

15. (Original) The apparatus of claim 14 wherein said timer is included within said computing device.

16. (Original) The apparatus of claims 14 where P_T is an integer multiple of P_n.

17. (Original) The apparatus of claim 14 wherein P_T is other than an integer multiple of P_n and $P_T >> P_n$.

18. (Original) The apparatus of claim 14 wherein said modulator further comprises overflow bit.

19. (Previously Presented) An apparatus improving the resolution of an n bit pulse width modulator having a P_n period, the apparatus comprising:

a timer to generate K timer states, wherein K is greater than 2 and having a timer period P_T;

a computing device for assigning a modulator output value to each of said K states; and

whereby said modulator outputs a plurality of pulses according to a modulator output value during each P_n period occurring within timer period P_T and whereby the pulse width modulator has a resolution of $n + \log_2 K$.

20. (Withdrawn) An LED backlit display comprising:

an array of LEDs;

an n bit pulse width modulator having a period of P_n;

a computing device for assigning a modulator output value to each of said K states;

whereby said modulator outputs a plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T and whereby said pulse width modulator has a resolution of $n + \log_2 K$.; and

a driver for supplying power to said array in accordance with said modulator output.

21. (Previously Presented) A method for improving the resolution of a hardware based pulse width modulator, the method comprising:

generating a pulse width modulated signal during a first time interval having a first modulator output; and

generating multiple further pulse width modulated signals during multiple succeeding time intervals having selected modulator outputs; and

repeating the generation of such pulse width modulated signals during the first and

succeeding time intervals to provide an overall duty cycle having a desired resolution higher than the resolution of the hardware based pulse width modulator.

22. (Previously Presented) A method for improving the resolution of a hardware based pulse width modulator, the method comprising:

specifying a desired duty cycle;

determining a timer state;

if the state needs to be set at 100% duty cycle, setting the duty cycle to 100%;

otherwise, setting pulse width modulation of the pulse width modulator to an appropriate value for this state;

turning off a 100% duty cycle bit; and

incrementing a state counter for a next state.

23. (Previously Presented) A system for improving the resolution of a hardware based pulse width modulator, the system comprising:

means for generating a pulse width modulated signal during a first time interval having a first modulator output; and

means for generating multiple further pulse width modulated signals during multiple succeeding time intervals having selected modulator outputs; and

means for repeating the generation of such pulse width modulated signals during the first and succeeding time intervals to provide an overall duty cycle having a desired resolution higher than the resolution of the hardware based pulse width modulator.